What Is Claimed Is:

1. A method to form a metal line structure on a substrate comprising:

forming first metal lines, the first metal lines having a first barrier metal layer and a first conductive layer;

forming a first interlayer insulator on the substrate and the first metal lines;

planarizing the first interlayer insulator by removing a part of the first interlayer insulator to expose a top surfaces of the first metal lines;

forming a second interlayer insulator on the first interlayer insulator and the first metal lines;

selectively etching the second interlayer insulator to expose top surfaces of the first metal lines;

sequentially forming a second barrier metal layer and a second conductive layer on the etched second interlayer insulator and the first metal lines; and

planarizing the second conductive layer and the second barrier metal layer to expose top surfaces of the second interlayer insulator, thereby forming second metal lines comprising a portion of the second barrier metal layer and a portion of the second conductive layer.

2. A method as defined in claim 1, wherein each of the first metal lines has about 50% of a desired thickness of a desired metal line structure.

3. A method as defined in claim 2, wherein the first metal lines comprise an Al alloy containing about 5% or less Cu.

4. A method as defined in claim 1, wherein a portion of each of the first metal line protruding from the first interlayer insulator is removed, after planarizing the first interlayer insulator.

5. A method as defined in claim 1, wherein the planarizing is performed by a CMP process.

6. A method as defined in claim 1, wherein the second interlayer insulator has about 50% of a desired thickness of a desired metal line structure.

7. A method as defined in claim 1, wherein the second conductive layer comprises Cu.

8. A method as defined in claim 1, wherein the first interlayer insulator is made of USG or FSG deposited by an HDP process.

9. A method as defined in claim 1, wherein the second interlayer insulator is made of USG or FSG deposited by a PECVD process.

10. A method as defined in claim 1, wherein the second interlayer insulator is made of USG or FSG deposited by PECVD SiOC.

11. A method as defined in claim 1, wherein the first and the second barrier metal layers comprise at least one of Ti, TiN, Ta, TaN, W and WN.

12. A metal line structure formed in a semiconductor device, comprising:

first metal lines formed on a substrate, the first metal lines having a first barrier metal layer and a first conductive layer;

a first interlayer insulator between adjacent ones of the first metal lines;

second metal lines formed on respective ones of the first metal lines, the second metal lines having a second barrier metal layer and a second conductive layer; and

a second interlayer insulator between adjacent ones of the second metal lines.

13. A metal line structure as defined in claim 12, wherein each of the first metal lines has about 50% of a desired thickness of the metal line structure.

14. A metal line structure as defined in claim 12, wherein the first metal lines comprises an Al alloy containing 5% or less.

15. A metal line structure as defined in claim 12, wherein the second interlayer insulator has about 50% of a desired thickness of the desired metal line structure.

16. A metal line structure as defined in claim 12, wherein the second conductive layer comprises Cu.

17. A metal line structure as defined in claim 12, wherein the first interlayer insulator is made of USG or FSG deposited by an HDP process.

18. A metal line structure as defined in claim 12, wherein the second interlayer insulator is made of USG or FSG deposited by a PECVD process.

19. A metal line structure as defined in claim 12, wherein the second interlayer insulator is made of USG or FSG deposited by a PECVD SiOC.

20. A metal line structure as defined in claim 12, wherein the first and the second barrier metal layers comprise at least one of Ti, TiN, Ta, TaN,

W and WN.